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The Single Event Upset Forecasting in Digital and Analog Integrated Circuits in SAED 14nm FinFet Technology

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***Abstract* — This paper presents a forecasting method of the Single Event Upset effect on the performance of analog and digital circuits designed in SAED 14nm FinFet technology. Meanwhile, the EDA tool was suggested which automatically inserts the radiation effect in the SPICE netlist and generates a new netlist for further debugging. The tool can automatically run a SPICE simulation and generate plot files in SPICE output formats. The suggested user-friendly GUI helps the designer to realize the measurements and organize the faster debug.**

***Keywords* — SAED 14nm FinFet; radiation; parametric degradation; single event upset; SPICE Compatible Single Event Upset Debugger; an incident particle; voltage overshoot.**

I. INTRODUCTION

Radiation-resistant electronics have been used in various areas. Generally, the aerospace, nuclear reactors, and military applications [1] use rad-hard integrated circuits (ICs) [2]. ICs operating in above-mentioned spheres operate under a large amount of radiation which is resulting in significant parametric degradations of the analog and digital circuits. Meanwhile, this effect can lead to unexpected current generations and voltage strikes that occur on analog and digital parts.

An example of the influence of radiation effects on IC functionality is presented in Fig. 1.

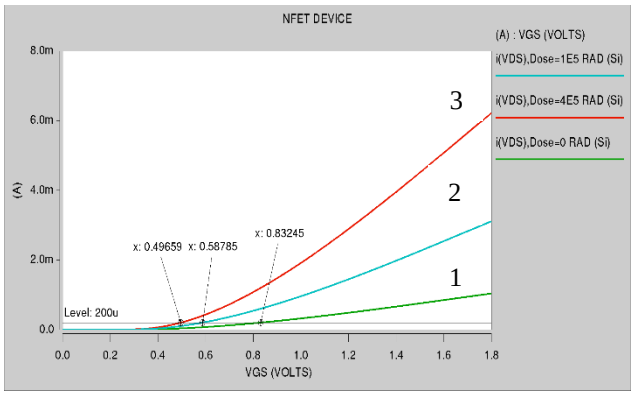


Fig. 1. Influence of radiation on transfer characteristics of NFET transistor

The dependency of the drain current on the gate-source voltage of NFET transistor is presented. The simulation was run with HSPICE simulator [3] and output plots are presented with Saber tool [4]. In the transfer characteristics before radiation effect is presented in the first curve. The second curve corresponds to the transfer characteristics of the transistor in 30kRad case. In the third curve, the radicalization dose was set to 100kRad. The threshold voltage shift was measured after the radiation effect [5]. According to the simulation results, it was decreased 2 times. The threshold shift is critical both in analog and digital ICs. In digital ICs it may cause high dynamic currents flowing through the digital cells during the transitions. In analog blocks, it causes current mismatches in current mirror block, the degradations of the parameters of operational amplifiers and op-amp based systems etc.

II. THE INFLUENCE OF SINGLE EVENT EFFECT ON THE PARAMETERS OF ANALOG AND DIGITAL CIRCUITS

The result of the single event effect (SEE) commonly takes place during the operation of the analog and digital parts of integrated circuits. The influence of the effect can appear on every transistor of the system, on the part of the IC or on whole IC. High energy particles cause huge violations and even force the IC to break down mode [6].

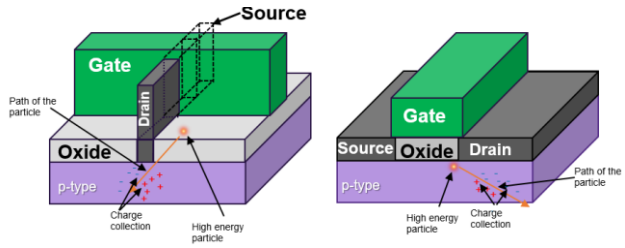
The most common type of errors meeting in ICs is single event upsets (SEU) effect. During this effect a path of electron-hole pairs forms which means that there is a charge collection after ion strike [7,8]. The collected charge can be calculated using Liner Energy Transfer (LET) phenomenon. Equation (1) is defined to calculate the energy transferred to the matter by the incident particle.

$$LET = 1/\rho \times dE/dx \qquad (1)$$

where ρ is the density of a material, dE ×dx is the energy that transferred to silicon on the path length, [LET] = $J \times m^2 \times kg^{-1}$ or [LET] = $MeV \times cm^2 \times mg^{-1}$ [6].

This may result in generation of incorrect transitions in digital integrated circuits or voltage shift in analog signals. In Fig. 2 the process of Single Event Effect is illustrated for MOSFET transistors and for FinFet transistors. If the collected charge causes SEU then the collected charge is the critical charge on which SEU can appear. Experimental data provide the importance of those effects. Until the LET

is equal to 10 MeV*cm^2/mg, the FinFet device shows higher stability than the MOSFET devices. With the increase of LET (close to 20MeV*cm^2/mg) the behaviour of FinFet devices became same as the MOSFET behavior [8].



(a) (b)

Fig. 2. Single Event Effect (SEE) in (a) FinFet transistor and (b) MOSFET transistor [7]

III. THE 14NM FINFET BANDGAP REFERENCE CIRCUIT

Consistent voltage references are necessary parts in precision analog designs. The process, supply voltage and temperature (PVT) variations are the main reasons which cause the output voltage variations of any voltage reference based on voltage regulators. The power supply can vary by ±10%. While in the precision systems like analog to digital converters (ADC) the reference voltage variation shouldn't exceed ±2-3%. Hence traditional voltage regulators don't work on those conditions due to the high variation of the supply voltage. The bandgap reference circuits are used to compensate these variations and achieve higher accuracies [9].

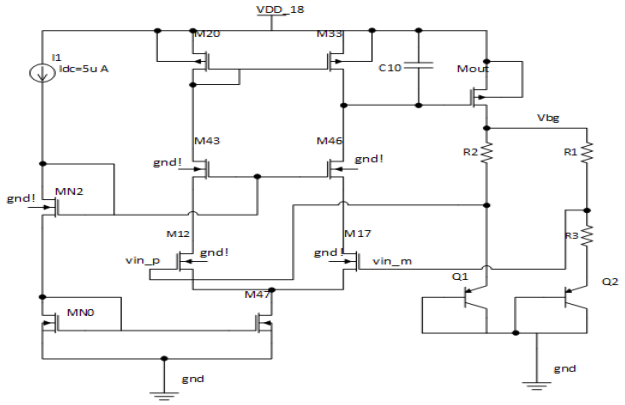


Fig. 3. Bandgap reference circuit

To achieve temperature independence of any system two opposite components are required. In bandgap references, the negative temperature coefficient derives from the base-emitter voltage of p-n junction of the diode-connected bipolar transistor.

Fig. 4 presents the dependency of base-emitter voltage on the temperature. The Negative to absolute temperature (NTAT) coefficient In SAED 14nm FinFet technology [10] variation is equal to 255mV.

$$NTAT = \frac{dV_{be}}{dT} = -1.5^{mV}/_{K}$$

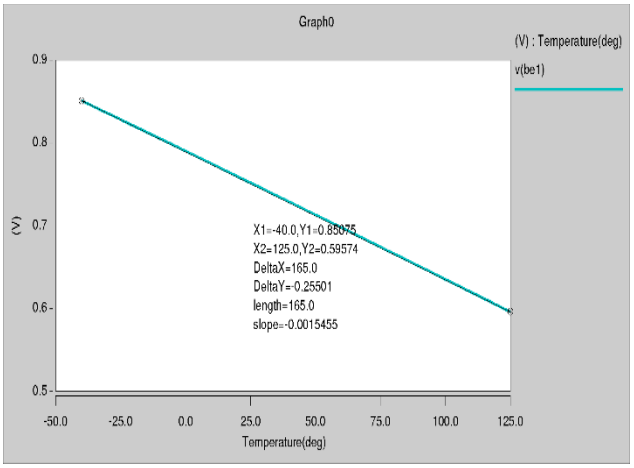


Fig. 4. The dependency of base-emitter voltage on the absolute temperature

The Positive to absolute temperature (PTAT) coefficient derives from the voltage difference of the two p-n junctions operating at unequal current densities.

$$PTAT = V_T * \ln\frac{n * I_0}{I_{s1}} - V_T * \ln\frac{I_0}{I_{s2}}$$

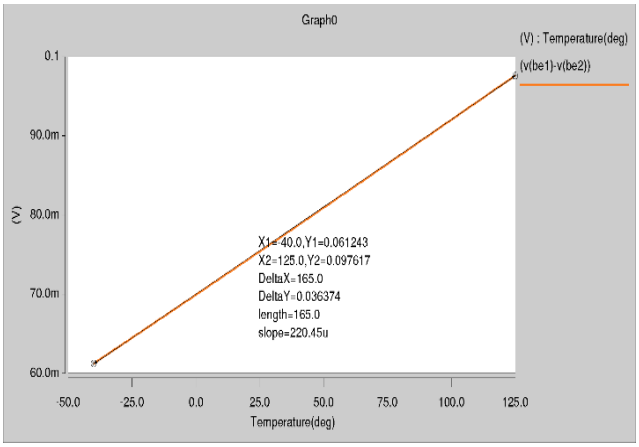


Fig. 5. Positive to absolute temperature dependency

The temperature dependency of the output reference voltage on the technology is presented in Fig. 6. In a typical case, the simulation results show less than 5mV dependency on the absolute temperature which varies in -40^{0}C to +125^{0}C range. The voltage independence will be achieved while the transistors operate in the saturation region. The simulation results, where the PVT parameters are varied, are presented in Table 1. The V_{bg} PVT variation is [1.1900 – 1.2160] i.e. 26mV while the supply voltage varies with 360mV.

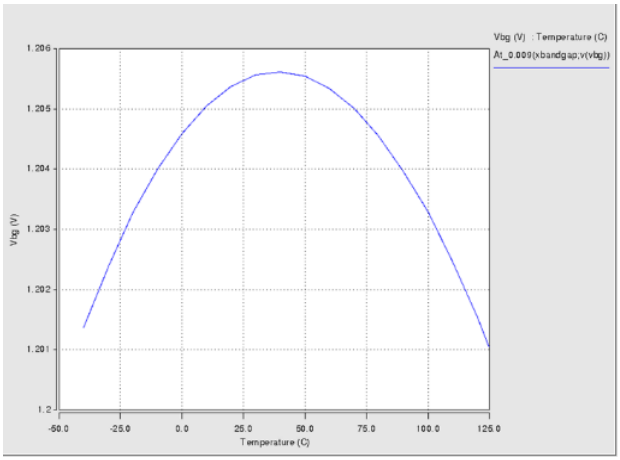


Fig. 6. Reference voltage vs absolute temperature

Table 1

Reference Voltage Variation vs PVT Variations

	TT/bip_t VDD18=1.8V	***SS/bip_s VDD18=1.62V***	***FF/bip_f VDD18=1.98V***
Vbgmin (V)	1.2010	1.1900	1.2102
Vbgmax (V)	1.2055	1.1960	1.2160
Vbg-40 (V)	1.2015	1.1915	1.2120
Vbg+125 (V)	1.2010	1.1900	1.2102

IV. THE DESCRIPTION OF SCSEU TOOL

SCSEUD EDA debugging tool is developed to organize the simulation of the SEU at transistor (or circuit) level. The benefits of the suggested tool are:

- Spice compatibility.
- Multiple Single Event Effect injection.
- Fast debug of the influence of SEU.
- High accuracy due to the SPICE compatibility.
- User-friendly simple GUI.

The benefits of suggested tool propose a new way of designing RadHard integrated circuits. It's a separate module which can be integrated with other tools.

SCSEU tool is written in C programming language. Apart from that, during the development of the tool, the C++/Qt5 libraries have been used to create user-friendly GUI [11]. The designer can provide the required information for SEU simulation by using the proposed GUI. Input file of the tool is a SPICE netlist. The tool works on the given netlist and as result provides an output which is a modified (SEUs injected) SPICE netlist file. In Fig. 7 the corresponding scenario is presented [12]. The (2) illustrates the current pulse function of time [13].

$$I(t) = Io * \frac{e^{-\frac{t}{\alpha}} - e^{-\frac{t}{\beta}}}{\cos(\theta)} \qquad (2)$$

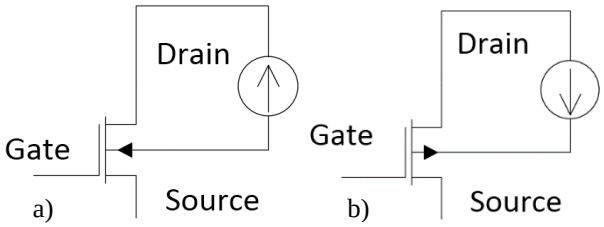


Fig. 7. The SPICE model of SEU on a) NFET transistor, b) PFET transistor

where I_o - is the maximum possible current, θ - is the angle of an incident particle to the surface of the circuit, α - is a collection time constant of the junction, and β - is the time constant of initial establishing the ion track. For SEAD14nm FinFet technology their values are equal to α=150ps and β=4ps. The approximate maximum current is nearly proportional to the energy of the particle. The total current goes up as the angle of the incident particle rises. The Single Event Upsets are injected into SPICE netlist. Two possible methods are suggested to the designer to choose whether random or manual method is preferable.

A. Randomly

This method is helpful in case there is a huge number of devices and it is not known which device has a higher influence on the simulation results. The first step of the tool is the gathering information from the given netlist. The tool passes through the netlist once and saves information such as wires, connection points, device names, device positions. SCSEU tool needs to know transistors types because SEU errors are injected differently depending on the transistor type. It searches for information about transistor model to determine its type. The information is gathered only for those devices that SEUs can be inserted on. Table 2 shows the types of devices that SEEs can be injected on.

Table 2

The list of supported types of devices and the schematic updates that SCSEU tool implements in the netlist

Device type	Schematic connection
NFET/PFET	drain to bulk
PNP/NPN	emitter to base and collector to base
N/P-type diode	cathode to anode
Interconnections	on the interconnection

The devices which are not supported by the tool (such as capacitors, inductors) will be automatically neglected by the tool. In random simulation case, the tool chooses the device on which the influence appears from the listed detailed information about the devices. Passing through the netlist once more the randomly chosen devices are found and SEUs are inserted. For example, on the transistors, the influences are injected by adding an exponential current source corresponding to the SEU radiation energy between the drain and the body. The random generation mechanism of SEU insertion in SPICE netlist organized by the GUI is presented in Fig. 8.

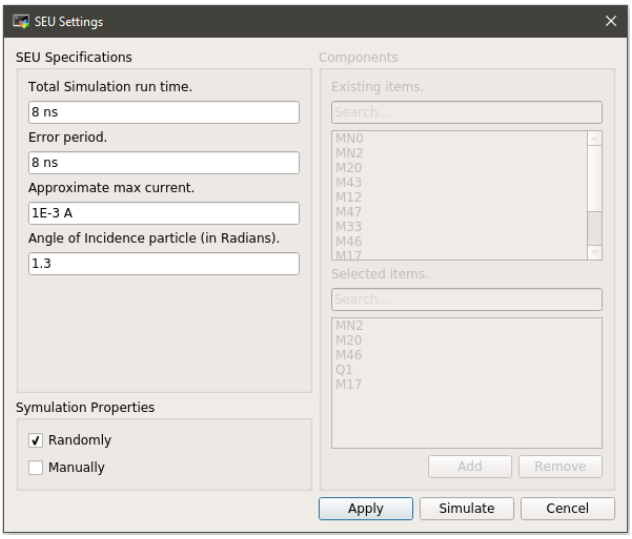


Fig. 8. SCSEUD random simulation GUI

B. *Manually*

To specify the names of the devices on which the SEU effect should be simulated, the separate GUI window is created (Fig. 9). In the *Existing items* window, the whole list of devices is listed. To select one from the list, the corresponding device should be selected and moved to the *Selected items* view.

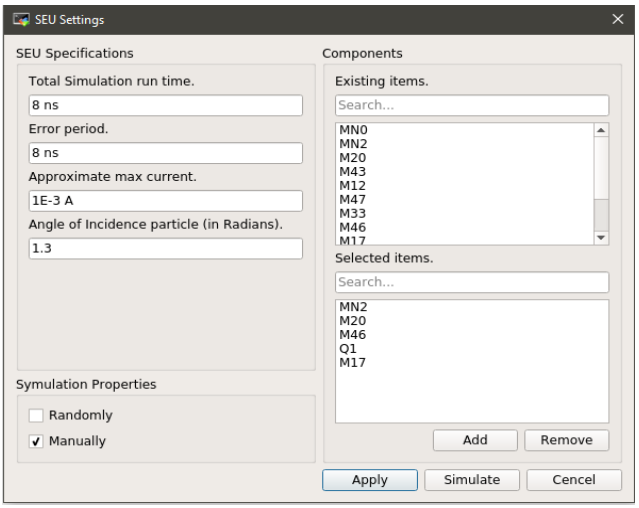


Fig. 9. SCSEUD manual simulation GUI

V. THE IMPACT OF SEU ON CMOS LATCH

The transient simulation results after the applied SEU at the output node of the CMOS latch is presented in Fig. 10 and Fig. 11. The peak current injected by the SEU was selected from 20uA to 90uA and the output voltage drops with 300mV from its initial "1" (800mV) value. This is close to the threshold voltage of the FinFet device and can lead to unexpected transition on the output of the next stage of the latch. Meanwhile, the dropped voltage can change the state of the latch to the "0" or force it to enter the metastable state.

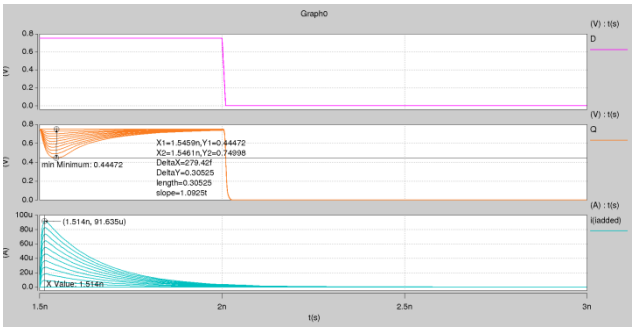


Fig. 10. The impact of SEU on CMOS latch while static "1" is stored

The same test was implemented with the latch stored "0" value. The 90uA injected current is enough to change the state of the latch and the 75uA current is enough to raise the stored voltage value with 300mV.

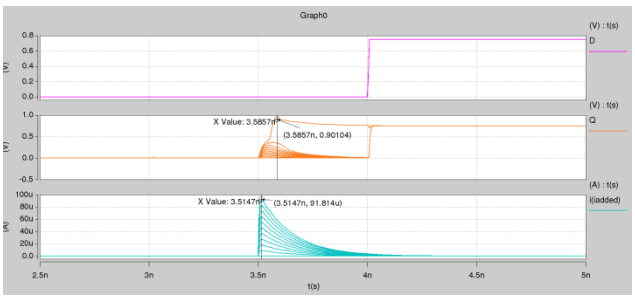


Fig. 11. The impact of SEU on CMOS latch while static "0" is stored

VI. THE IMPACT OF SEU ON THE PERFORMANCE OF BANDGAP REFERENCE

To estimate the influence of the SEU on the performance of the bandgap reference the manual method was selected. SPICE simulation was run with HSPICE. The peak current injected by the SEU was selected from 20uA to 90uA and the output voltage strikes were plotted. First, the SEU was applied to the bipolar transistor Q1. Fig. 12 presents the simulation results. In 90uA case the positive strike value is equal to 1.22V which also can cause voltage overshoots and stress conditions for the low voltage FinFet devices.

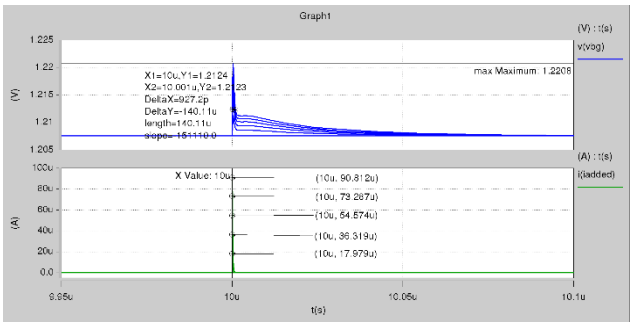


Fig. 12. The impact of SEU on Q1 bipolar transistor

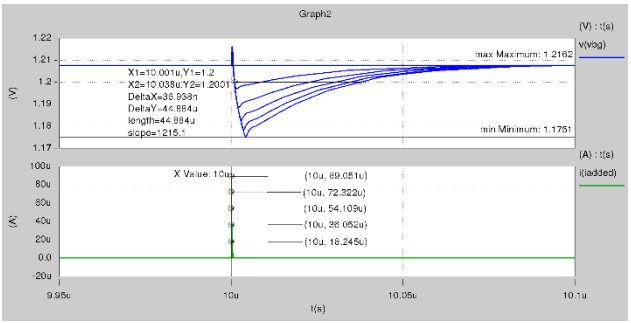


Fig. 13. The impact of SEU on M12 input transistor

Then the simulation has been implemented by applying the SEU on M12 input device (Fig13). The injected current causes a voltage drop at the output. The voltage drop is approximately 40mV. Bandgap output settles to its nominal value after 37ns. The final check has been implemented on Mout device (Fig. 14). Again, output voltage overshoot is detected.

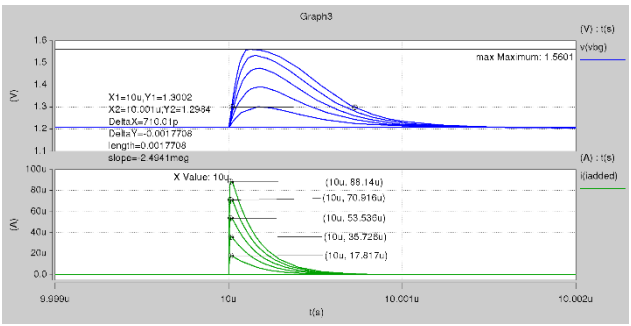


Fig. 14. The impact of SEU on Mout transistor

VII. CONCLUSION

The single event upset forecasting method in analog and digital circuits designed with SAED 14nm FinFet technology is proposed in this paper. To estimate the influence of the SEU digital and analog blocks have been discussed. The FinFet latch was designed and the forecasting of radiation effect on the stability of the latch was measured. The bandgap reference circuit with PVT compensation is designed and SEU effect simulation was implemented to measure the performance of the analog-sensitive parts. Meanwhile, the Spice Compatible Single Event Upset Debugger (SCSEUD) tool was developed to realize the SPICE netlist update and run SPICE simulation to analyze the SEU effect on the performance of analog and digital circuits

REFERENCES

[1] H. Spieler, Introduction to radiation-resistant semiconductor devices and circuits. InAIP Conference Proceedings 1997 Jan 25 (Vol. 390, No. 1, pp. 23-49). AIP.

[2] G. Roosevelt, W. Roper and T. Romanko, "Optimizing high speed serial communication using Honeywell Rad Hard SerDes," 2011 NASA/ESA Conference on Adaptive Hardware and Systems (AHS), San Diego, CA, 2011, pp. 215-219.

[3] HSPICE Reference Manual, Synopsys Inc.- 2017. -846p.

[4] Saber Reference Manual, Synopsys Inc.- 2017. -312p.

[5] F. Faccio, G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2413-2420, Dec. 2005.

[6] P. Malinowski, "Design of Radiation Tolerant Integrated Circuits", MSc thesis, Technical University of Lodz, 2006

[7] S. Lee, I. Kim, S. Ha, C.-S. Yu, S. Pae, J. Noh, and J. Park, “Radiation induced soft error rate analyses for 14 nm FinFET SRAM devices,” in Proc. IEEE Int. Rel. Phys. Symp., Apr. 2015, pp. 4B.1.1–4B.1.4.

[8] P. Nsengiyumva et al., “A comparison of the SEU response of planar and FinFET D flip-flops at advanced technology nodes,” IEEE Trans. Nucl. Sci., vol. 63, no. 1, pp. 266–272, Feb. 2016.

[9] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York, NY USA, 2001. p. 306,

[10] V. Melikyan, M. Martirosyan, G. Piliposyan, 14nm Educational Design Kit: Capabilities, Deployment and Future, Small Systems Simulation Symposium 2018.

[11] URL:http://doc.qt.io/qt-5/reference-overview.html (access date: 01.05.2018)

[12] K. KleinOsowski, AJ. KleinOsowski, D. J. Lilja, The SEASONing Tool: A Spice Engine for Adding Soft-errors On Netlists, University of Minnesota Laboratory for Advanced Research in Computing Technology and Compilers Technical Report No. ARCTiC 05-09, May, 2005.

[13] URL:http://www.pspice.com/resources/application-notes/radiation-effect-modeling (access date: 01.05.2018)

Прогнозирование одиночного сбоя в цифровых и аналоговых интегральных схемах по технологическому процессу SAED 14nm FinFet

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***Аннотация* — Одним из факторов, влияющих на стабильность интегральных схем, является наличие радиации в окружающей среде. Влияние радиации становится критическим в случае использования интегральных схем в системах работающих в условиях интенсивного радиационного фона. К примеру, в**

системах используемых в космосе, в военной технике, в ядерной промышленности. В рамках данной статьи было разработано программное обеспечение (ПО) Spice-Compatible-Single-Event-Upset-Debugger (SCSEUD), которое обеспечивает быстрое моделирование одиночных сбоев в ИС. На вход данного ПО подаётся файл, описанный на языке SPICE (SPICE netlist). На выходе получаем файл того же типа, но уже с учетом влияния воздействия радиационного эффекта одиночного сбоя, при моделировании которого получаем возможность измерить воздействие радиационного эффекта.

Основными элементами ИС являются узлы статической памяти, к коим относятся триггеры. Под воздействием радиации в данных устройствах могут возникнуть состояния метастабильности и ложные переключения.

В данной исследовательской работе с помощью программного обеспечения было выполнено прогнозирование воздействия радиации на цифровой узел – D-триггер. Была определена минимальная доза радиации, воздействие которой вызывает изменение абсолютного значения выходного напряжения триггера больше чем на значение порогового напряжения транзистора (0,3 В). Данной дозы воздействия достаточно для введения триггера в состояние метастабильности или для его переключения. При разработке аналоговых интегральных схем используются узлы, в которых необходимо применение источников стабильного напряжения. Примерами таких схем являются аналого-цифровые преобразователи, компараторы и т.д. В вышеуказанных системах допустимая погрешность не должна превышать ± 2-3%. Таким образом, использование источников питания или стабилизаторов напряжения в качестве генераторов стабильного опорного напряжения становится невозможным, поскольку диапазон погрешности данных систем составляет ± 10%.

Возникает задача разработки размещаемых на кристалле источников стабильного опорного напряжения. Примером такой системы является источник опорного напряжения (ИОН), выходное напряжение которого равно ширине запрещённой зоны используемого полупроводника. Источник такого типа обеспечивает независимость получаемого опорного напряжения от процесса, напряжения питания и температуры.

В рамках данного исследования по технологическому процессу SAED 14nm FinFet был разработан источник опорного напряжения с номинальным значением 1.2В. В свою очередь, отклонение от номинального значения в зависимости от процесса, напряжения питания и температуры составляет 26мВ.

Используя данное программное обеспечение было произведено прогнозирование влияния сбоя. Из результатов следует, что вследствие радиационного воздействия на ИОН возникают отклонения значения номинального напряжения – падение или возрастание в зависимости от дозы радиационного воздействия и от конкретного элемента подвергающегося воздействию.

***Ключевые слова* — SAED 14nm FinFet; радиация; деградация параметров; одиночный сбой; SPICE Compatible Single Event Upset Debugger; заряженная частица; перенапряжение.**

ЛИТЕРАТУРА

[1] H. Spieler, Introduction to radiation-resistant semiconductor devices and circuits. InAIP Conference Proceedings 1997 Jan 25 (Vol. 390, No. 1, pp. 23-49). AIP.

[2] G. Roosevelt, W. Roper and T. Romanko, "Optimizing high speed serial communication using Honeywell Rad Hard SerDes," 2011 NASA/ESA Conference on Adaptive Hardware and Systems (AHS), San Diego, CA, 2011, pp. 215-219.

[3] HSPICE Reference Manual, Synopsys Inc.- 2017. -846p.

[4] Saber Reference Manual, Synopsys Inc.- 2017. -312p.

[5] F. Faccio, G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2413-2420, Dec. 2005.

[6] P. Malinowski, "Design of Radiation Tolerant Integrated Circuits", MSc thesis, Technical University of Lodz, 2006

[7] S. Lee, I. Kim, S. Ha, C.-S. Yu, S. Pae, J. Noh, and J. Park, “Radiation induced soft error rate analyses for 14 nm FinFET SRAM devices,” in Proc. IEEE Int. Rel. Phys. Symp., Apr. 2015, pp. 4B.1.1–4B.1.4.

[8] P. Nsengiyumva et al., “A comparison of the SEU response of planar and FinFET D flip-flops at advanced technology nodes,” IEEE Trans. Nucl. Sci., vol. 63, no. 1, pp. 266–272, Feb. 2016.

[9] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York, NY USA, 2001. p. 306,

[10] V. Melikyan, M. Martirosyan, G. Piliposyan, 14nm Educational Design Kit: Capabilities, Deployment and Future, Small Systems Simulation Symposium 2018.

[11] URL:http://doc.qt.io/qt-5/reference-overview.html (access date: 01.05.2018)

[12] K. KleinOsowski, AJ. KleinOsowski, D. J. Lilja, The SEASONing Tool: A Spice Engine for Adding Soft-errors On Netlists, University of Minnesota Laboratory for Advanced Research in Computing Technology and Compilers Technical Report No. ARCTiC 05-09, May, 2005.

[13] URL:http://www.pspice.com/resources/application-notes/radiation-effect-modeling (access date: 01.05.2018)