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Layout Dependent Effects Impact on Standard Cells Layout in 28 nm Technology Node

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Abstract **— Impact of Layout Dependent Effects (LDE) on timing and power characteristics of standard cells becomes more critical in deep-submicron technologies. In this article different types of LDE parameters have been studied - Well Proximity Effect (WPE), Poly Spacing Effect (PSE), Length Of Diffusion (LOD), Oxide Spacing Effect (OSE). The set of test layouts have been developed to define impact of LDE parameters in 28 nm standard cells. Layout parasitic netlists for every test layout have been simulated to identify the changes of timing and power characteristics. Also, additional cells with the same functionality but with different layout implementation have been added in a library and logic synthesis for a test design have been implemented. Based on cell-level simulations and logic synthesis results for the test design the set of recommendations have been provided.**

Keywords **— Layout Dependent Effects (LDE), Well Proximity Effect (WPE), Poly Spacing Effect (PSE), Length Of Diffusion (LOD), Oxide Spacing Effect (OSE).**

I. INTRODUCTION

With scaling technology nodes, Layout Dependent Effects (LDE) become an important problem which must be taken into account during standard cell libraries development. These effects can significantly impact on the parameters of the transistors and correspondingly on power and timing characteristic of standard cells.

One of the major issues in modern CMOS technology is the dependency of a cell performance on layout [1, 2]. The main reasons of LDE are proximity effects and various mechanical stresses caused by the technological process. The basic sources of LDE are described in [3-5] and shown in Fig. 1.

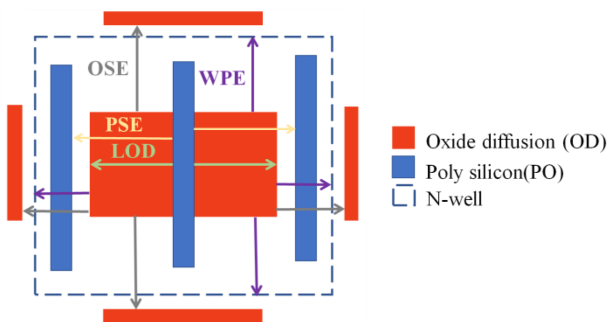

Fig. 1. Main sources of LDE

All these parameters are usually included in modern transistor models and can be obtained by extraction from the layout in the netlist with interconnects and parasitic parameters [6].

II. LDE: Impact on Cell Average Switching Delay and Average Leakage Current

LDE parameters cannot be completely excluded from the layouts due to density and minimal area requirements for standard cells. Simulation flow with Layout Parasitic Extraction (LPE), illustrated in Fig.2, has been used for proper taking these parameters into account.

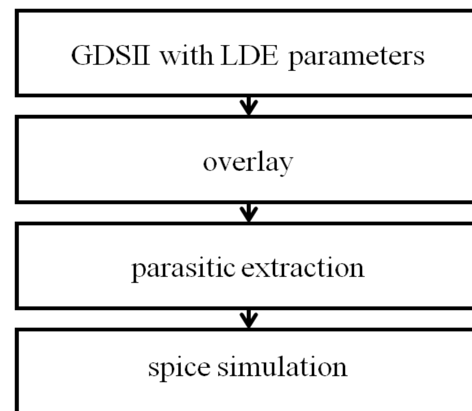

Fig. 2. Simulation flow to investigate impact of LDE

High speed library (12 metal track height and 30 nm gate length) in 28 nm technology node was chosen for investigation.

Traditionally, on the SoC level all standard cells are placed in rows together with other cells and higher level routing metals. Proximity of surrounded cells significantly impacts on cell characteristics. For more accurate simulations it is recommended to emulate real placement and environment for a cell before Layout Parasitic Extraction (LPE). Therefore the special overlay structure, presented in Fig. 3, has been used.

The main idea of the overlay structure is the following: layout of tested cell is surrounded by dummy Oxide Diffusion (OD) and poly-gate layers which reproduce placement in real rows. «Metal Grid» over the tested cell layout emulates external routing to make result of netlist with parasitic parameters more realistic.

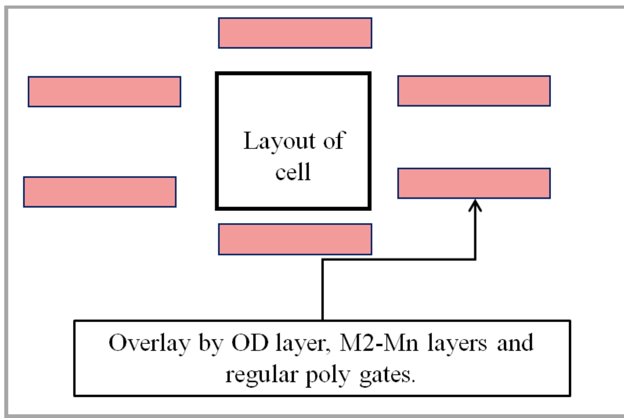

Fig. 3. Overlay structure for Layout parasitic Extraction to generate a netlist with parasitic parameters

When LPE netlist is generated, the Spice simulation can be run. General scheme for modeling the netlist with parasitic parameters is shown in Fig. 4.

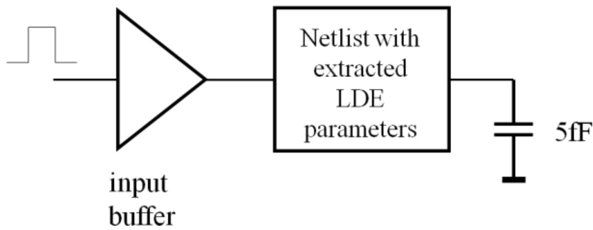

Fig. 4. General scheme for modeling the netlist with parasitic parameters

Two measurements should be performed to define average leakage current: the leakage current «1» through the PMOS transistor and leakage current «0» through the NMOS transistor. Correspondingly, the input logic values «0» or «1» were applied on a time interval from 0 to 100 ns. Leakage current values were measured in a point of 50 ns.

Timing and power characteristics have been defined for layouts of such logic cells as INV, NAND2 and NOR2 with minimal driving strength. In this case the transistors in the complementary pair have the smallest widths, that allow changing layouts of a test cell without area increase, correspondingly investigating impact of LDE parameters.

A. WPE Simulations

In the current CMOS processes, wells are usually created using high energy ion implantation which requires a thick photoresist layer to mask the well implants. Ions, which are implanted into the edge of the photoresist, can be propagated laterally into an adjacent region of a transistor.

Channel implant dopant and well implant dopant have the same type, therefore the additional doping increases the absolute value of the threshold voltage of both NMOS and PMOS devices [5].

Five test layouts, illustrated in Fig. 5, were developed to determine WPE impact on the characteristics of INV.

In the first test structure (test1) the boundary of N-well is placed with maximum distance from PMOS transistor and with minimal distance from NMOS transistor.

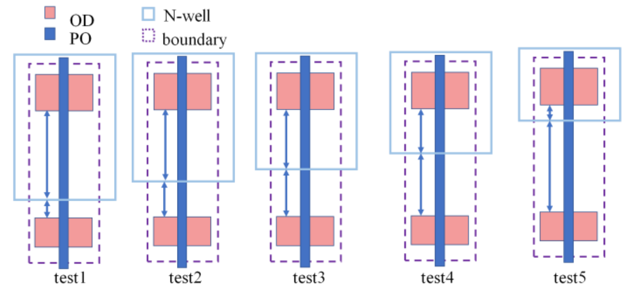

Fig. 5. Test layouts for investigation of WPE impact on timing and leakage power characteristics of inverter

In the second, third and fourth test structures the boundary of N-well is shifted in direction from NMOS transistor to PMOS transistor. Such, the distance from N-well boundary to PMOS transistor is decreasing consistently.

In the fifth test structure (test5) the boundary of N-well is placed with minimal distance from PMOS transistor and with maximum distance from NMOS transistor.

Selected combination of test structures, pointed in Fig. 5 allows to better analyze impact of N-well proximity on parameters of transistors.

The simulation results of all five test structures are presented in Table 1 and Table 2.

Table 1

WPE: Timing characteristics of INV

	test1	test2	test3	test4	test5
Delay rise, ps	21,507	21,625	21,801	22,230	23,229
Delay fall, ps	19,923	19,590	19,408	19,165	19,032
Average switching delay, ps	20,715	20,607	20,604	20,697	21,130

Table 2

WPE: Leakage currents for INV

	test1	test2	test3	test4	test5
Leakage current «1», uA	1,008	0,975	0,919	0,805	0,612
Leakage current «0», uA	1,470	1,617	1,713	1,846	1,918
Average leakage current, uA	1,239	1,296	1,316	1,326	1,265

The data in Table 1 show dependency for PMOS and NMOS transistors on distance to the edge of N-well. To minimize Delay rise (switching from «0» to «1» level) the distance between PMOS and the edge of N-well should be as maximum as possible. And conversely, to minimize Delay fall (switching from «1» to «0» level) the distance between NMOS transistor and N-well should be as minimum as it is allowed by Design Rule Manual (DRM). Thus, to minimize average delay for INV cell the distances

to NMOS and PMOS should be approximately equal or the edge of N-well should be located in the middle of cell.

Leakage simulation results, pointed in Table 2, show impact of WPE on PMOS and NMOS transistors.

If logic «1» is applied to the input then NMOS transistor is in active state, whereas PMOS transistor is closed and has the leakage current. Decreasing the distance between PMOS and the edge of N-well reduces Leakage current of PMOS transistor.

If logic «0» is applied to the input then PMOS transistor is in active state, whereas NMOS transistor is closed and has the leakage current. Decreasing the distance between NMOS and the edge of N-well reduces Leakage current of NMOS transistor.

For 28 nm technology the leakage current through NMOS is much bigger than through PMOS transistor due to higher mobility of electrons. Therefore minimal space between NMOS and N-well provides minimal average leakage current.

Similar conclusions are confirmed during WPE impact investigation for NAND2 and NOR2 gates.

B. PSE Simulation

Poly Spacing Effect (PSE) is caused by the distance between the polysilicon layers and affects the electrical parameters of the transistor, e.g. the drain current [2].

Standard cells in the given 28 nm technology have a 140 nm poly pitch. The design rules allow to have channel lengths of 30, 35 and 40 nm without poly pitch change. The cells with gate length 30 nm allow to investigate PSE for two different poly spacings – 105 nm and 110 nm. Correspondingly, two test layouts with different distances from dummy poly to the gate, illustrated in Fig. 6, have been developed.

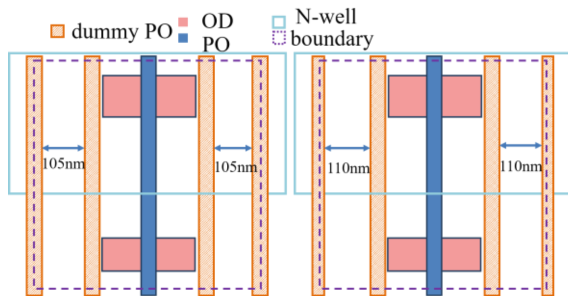

Fig. 6. Test layouts for PSE impact investigation

The simulation results of these structures are presented in Table 3 and Table 4.

Table 3

PSE: Timing characteristics of INV

	110nm	105nm	%
Delay rise, ps	21,801	21,803	0,009
Delay fall, ps	19,408	19,409	0,005
Average switching delay, ps	20,604	20,606	0,009

Table 4

PSE: Leakage currents for INV

	110nm	105nm	%
Leakage current «1», uA	0,919	0,919	0,000
Leakage current «0», uA	1,713	1,713	0,000
Average leakage current, uA	1,316	1,316	0,000

Simulation results (Table 3 and Table 4) for PSE on two test structures for INV cell show negligible impact on timing characteristics and zero impact on leakage currents. Thus PSE can be disregarded for standard cells development in this particular technology. The same results were obtained during PSE impact investigation for NOR2 and NAND2 gates.

C. LOD Simulation

For planar devices, LOD effect is mainly caused by Shallow Trench Isolation (STI). In Spice models BSIM4 this effect is well modeled. Device parameters of LOD are defined as spacing between gate edge and edge of OD [7].

In the given 28 nm technology the design rules allow to have two LOD values: 75 nm or 80 nm. In the first test structure (p80_n80) the LOD parameters of NMOS and PMOS transistors are equal to 80 nm. In the second and the third test structures (p80_n75, p75_n80) the LOD parameters of PMOS and NMOS were changed from 75 nm to 80 nm between each other. In the fourth test (p75_n75) the LOD parameters of both transistors are equal to 75 nm.

Test layouts to define the LOD effect are shown in Fig. 7. The results of circuit modeling are given in Table 5 and Table 6.

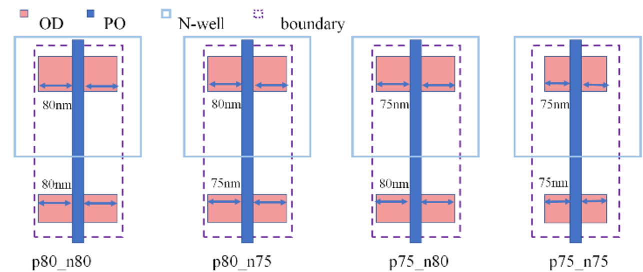

Fig. 7. Test layouts for LOD effect investigation

Table 5

LOD: Timing characteristics for INV

	p80_n80	p80_n75	p75_n80	p75_n75
Delay rise, ps	21,801	21,798	22,371	22,362
Delay fall, ps	19,408	19,465	19,376	19,430
Average switching delay, ps	20,604	20,631	20,873	20,896

Extension of OD for PMOS and NMOS transistors from Polysilicon gates allows to decrease both types of delay (Table 5). To minimize average switching delay the edge of OD should be extended on maximum distance from Poly gates of both transistors.

Table 6

LOD: Leakage currents for INV

	p80_n80	p80_n75	p75_n80	p75_n75
Leakage current «1», uA	0,919	0,919	0,899	0,899
Leakage current «0», uA	1,713	1,690	1,733	1,709
Average leakage current, uA	1,316	1,3044	1,316	1,3038

The data in Table 6 show that leakage current reduction for NMOS and PMOS transistors can be achieved by decreasing of distance between the edge of OD and Poly gates.

The same impact of LOD effect is confirmed by simulations on NAND2 and NOR2 gates.

D. OSE Simulation

The MOS characteristics will be impacted by OSE. The reason of this is the varying levels of STI mechanical stress caused by differences in OD space. At large STI widths, the effect of the neighboring OD region becomes negligible [5].

To investigate impact of OSE parameters on the characteristics of NMOS and PMOS transistors, ten test layouts have been developed according to Fig. 8 and Fig. 9.

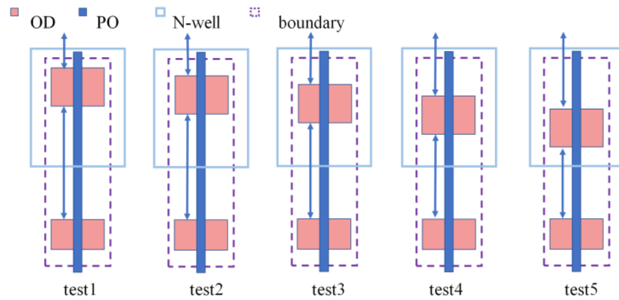

Fig. 8. Test layouts to investigate impact of OSE

First, with the optimal layout arrangement determined from the previous steps, NMOS is fixed whereas PMOS is shifted. In the first test structure (test1) the PMOS and NMOS are placed with maximum distance between each other.

In the second, third and fourth test structures the PMOS transistor is shifted in direction to NMOS transistor. Such, the distance from NMOS to PMOS transistors is decreasing consistently.

In the fifth test structure (test5) the PMOS transistor is placed with minimum distance to the N-well edge and NMOS transistor.

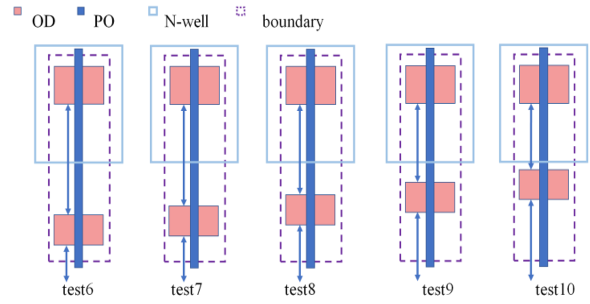

Fig. 9. Test layouts for determining the dependence of cell characteristics on OSE parameters

Then, PMOS is fixed, NMOS is shifted. In the sixth test structure (test6) the PMOS and NMOS are placed at maximum distance between each other. Note that test1 and test6 have identical layouts and are used as a reference for consistent comparison.

In the seventh, eighth, ninth test structures the NMOS transistor is shifted in direction to PMOS transistor. Such, the distance from NMOS to PMOS transistors is decreasing consistently.

In the tenth test structure (test10) the NMOS transistor is placed with minimum distance to the N-well edge and PMOS transistor.

The simulation results for INV are presented in Table 7 - 10.

Table 7

OSE: Timing characteristics of INV

	test1	test2	test3	test4	test5
Delay rise, ps	21,801	22,648	23,018	23,290	23,567
Delay fall, ps	19,408	19,394	19,388	19,374	19,350
Average switching delay, ps	20,604	21,021	21,203	21,332	21,459

Table 8

OSE: Timing characteristics for INV

	test6	test7	test8	test9	test10
Delay rise, ps	21,801	21,811	21,765	21,682	21,618
Delay fall, ps	19,408	19,613	19,750	19,858	19,891
Average switching delay, ps	20,604	20,712	20,758	20,770	20,755

Table 7 shows simulation results for the first group of the test structures. In this case the minimum of Delay rise is caused by maximum distance from PMOS to NMOS transistors and minimum spacing to dummy OD in overlay, which emulates active PMOS transistors in above placed row of standard cells. Delay fall difference is negligible because different distance to PMOS has small impact on

NMOS transistor. The first test structure (test1) has also minimum of average switching delay.

Timing characteristic results in Table 8 demonstrate timing dependency on OSE for the next five test structures. Reducing of Delay fall can be achieved by increasing distance to PMOS and decreasing spacing to dummy OD in overlay, which emulates active NMOS in below placed row of standard cells. Average switching delay is minimum in test6.

Table 9

OSE: Leakage currents for INV

	test1	test2	test3	test4	test5
Leakage current «1», uA	0,919	0,852	0,800	0,753	0,705
Leakage current «0», uA	1,713	1,711	1,706	1,700	1,690
Average leakage current, uA	1,316	1,281	1,253	1,226	1,198

In the first group of the test structures test5 has minimum leakage current values for both types of leakage (Table 9). Such result is caused by minimum distance from PMOS to NMOS transistor below and maximum spacing to dummy OD in overlay of above placed row of standard cells.

Table 10

OSE: Leakage currents for INV

	test6	test7	test8	test9	test10
Leakage current «1», uA	0,919	0,923	0,927	0,933	0,936
Leakage current «0», uA	1,713	1,660	1,607	1,582	1,552
Average leakage current, uA	1,316	1,291	1,267	1,257	1,244

For the next five test structures the minimum of leakage current «0» corresponds to test10 (Table 10), where NMOS transistor is located as close as possible to PMOS and has maximum spacing to dummy OD in overlay.

III. Recommendations to minimize LDE based on cell-level simulations

Based on cell-level simulation results the impact of WPE, PSE, LOD, OSE on the standard cell characteristics was identified. That allowed to define recommendations for standard cell layout development, depending on the timing and power requirements.

To reduce average switching delay of a cell it is recommended:

- to increase the distance from the edge of the N-well to the edge of the transistors (>>65 nm), that will reduce impact of WPE;
- to keep distance from the gate edge to horizontal transistor boundary (80 nm and more if possible), that will reduce impact of LOD;
- to place transistors as far away from each other as possible inside the cell (>>80 nm), that will reduce impact of OSE;

To reduce average leakage current it is necessary:

- to increase the distance from the edge of the N-well to the edge of the transistors (>>65 nm), that will reduce impact of WPE;
- to keep the distance from the gate edge to the vertical border of the transistor (75 nm and less if possible), that will reduce impact of LOD;
- place transistors as close to each other as possible inside the cell (OSE >= 80 nm).

IV. Logic synthesis results with new added cells, implemented to minimize impact of LDE

To further investigate impact of LDE in standard cells on power and timing characteristics at the synthesis stage, the test design was synthesized based on 28 nm standard cell library for Standard Voltage Threshold (SVT) option and 30 nm gate length.

Recommendation, given in Chapter 3, were applied to thirty most-used cells of the 28 nm library [8]. Correspondingly, two additional SVT libraries for High performance (HP) and for Low power (LP) options were developed with these additional cells [9]. Note, the area of new developed cells was the same as for the existing cells with the same function in the library.

The test design (~5K gates) was synthesized with two new LDE-optimized libraries («SVT30_HP» and «SVT30_LP») to define if there are some benefits for timing and power parameters.

The logic synthesis results for HP libraries are presented in Table 11. Column «SVT30» shows maximum achieved frequencies with the usage of initial «SVT30» library only. Column «SVT30_HP» demonstrates maximum achieved frequencies with the usage of both libraries - initial «SVT30» and new LDE-optimized «SVT30_HP», which includes 30 High performance modified cells.

Comparison results point, that even 30 LDE-optimized cells give small benefit (~1%) for timing characteristics without any penalty for design area.

Table 11

Comparison of maximum frequencies after synthesis with the SVT30_HP library and the SVT30 library

Target freq., MHz	Real freq, MHz		
	SVT30	SVT30_HP	%
50	117,6	118,6	0,8
100	175,7	177,6	1,1
150	212,5	214,4	0,9
200	236,9	238,4	0,6

The logic synthesis results for LP libraries are presented in Table 12. Column «SVT30» shows leakage power values for defined target frequencies with the usage of initial «SVT30» library only. Column «SVT30_LP» presents leakage power values with the usage of both libraries -initial «SVT30» and new «SVT30_LP» LDE-optimized, which includes 30 Low power modified cells.

Similar to previous results, the comparison demonstrates, that even 30 LDE-optimized cells give small benefit (~2%) for leakage power characteristics without any penalty for design area.

Table 12

Comparison of leakage power after synthesis with the SVT30_LP library and the SVT30 library

Target freq., MHz	Leakage power, mW		
	SVT30	SVT30_HP	%
50	1,691	1,661	-1,8
100	1,691	1,661	-1,8
150	1,692	1,662	-1,8
200	1,697	1,668	-1,7

V. CONCLUSION

LDE impact on timing and power characteristics of standard cells for 28 nm technology node has been analyzed in this article. A number of different layouts for test cells have been developed to study impact of different types of layout dependent effects – WPE, PSE, LOD, OSE.

Recommendations for layout dependent effects suppression have been proposed. Based on these recommendation two LDE-optimized libraries have been developed – High performance and Low power.

Logic synthesis of the test design (~5K gates) has been implemented with and without new additional libraries. The synthesis results showed small benefit on leakage power and timing without any area penalty in case the recommendation for LDE suppression were taken into account.

Proposed recommendations for LDE suppression in standard cells can be applied and taken into account during layout development stage, that will give additional small benefit on power and performance with zero drawback for area.

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Исследование влияния LDE на выбор топологии стандартных ячеек по технологии 28 нм

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***Аннотация* — Влияние эффектов, зависящих от топологии (LDE), на временные и мощностные характеристики стандартных ячеек становится важной проблемой в субмикронных технологиях. В данной статье**

исследованы различные параметры LDE: эффект близости кармана (WPE), эффект расстояния между кремниевыми затворами (PSE), эффект длины области диффузии (LOD), эффект расстояния между активными областями транзисторов (OSE). Для определения влияния параметров LDE на стандартные ячейки по технологии 28 нм был разработан набор тестовых топологий. Для определения изменений временных и мощностных характеристик были получены файлы с экстракцией из топологий. Кроме того, в библиотеку были добавлены дополнительные ячейки с той же функциональностью, но с измененной топологией, а также реализован логический синтез для тестового проекта. На основе результатов моделирования ячеек и логического синтеза тестового проекта был представлен набор рекомендаций по разработке топологий стандартных ячеек.

Ключевые слова **— эффекты, зависящие от топологии (LDE), эффект близости кармана (WPE), эффект расстояния между кремниевыми затворами (PSE), эффект длины области диффузии (LOD), эффект расстояния между активными областями транзисторов (OSE).**

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