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Complex Standard Cells Design Features in Advanced FinFET Technologies

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***Abstract* — A continuous scale of planar CMOS technology results in the development of new techniques for deep submicron processes or advanced nodes. A Fin Field-Effect Transistor (FinFET) device technology becomes one of the main trends as design rules are moving to 16nm and beyond. Providing many opportunities and advantages for IC design the FinFET technology raises a lot of questions regarding reusing of current design methodology, tools, and flows. While EDA vendors do not propose any groundbreaking approach to SoC design for advanced nodes, the FinFET technology should be effectively adapted to the existing design flow with an appropriate tuning. This article provides an overview of the main challenges of using 16nm FinFET technology for standard cells design, which are an essential part of any digital flow. General recommendations for standard cells design with FinFET technology are formulated. Features of complex cells design with applying of multi-height layout architecture are presented. The proposed guidelines were proven on the example of multi-bit flip-flops design providing area effective solution for low power applications.**

***Keywords* — FinFET technology, advanced node, digital library, standard cell library, logic library, low power standard cell, multi-height layout architecture, multi-bit flip-flop.**

I. INTRODUCTION

Even though original concept of vertical multi-gate MOSFET device was proposed a quite long time ago in 1989 [1], a widespread adoption as production technology FinFET structures got relatively recently. The FinFET technology was developed by leading semiconductor foundries as demand on emerged issues of planar MOSFET process with scaling to deep submicron sizes. Over the period of 2011 to 2014, the technology node was introduced by key industry players like Intel, Samsung, and TSMC [2], [3]. It is worth pointing that there are numerous different gate structures evolved from planar devices in three-dimensional devices, which possess various characteristics and features [1], [4]. The article is focused on so-called shorted-gate (SG) bulk FinFET devices compatible with planar MOSFET technology that results in lower fabrication cost and rapid deployment to manufacturing due to bulk substrate usage [5].

A. General bulk FinFET definition

A key concept of the innovative technology is a three-dimensional device structure also called tri-gate consisting of thin silicon fins that form the source and drain regions of the FinFET transistor and providing the channel for current to flow in the open state [3], [6]. A poly gate is wrapped around vertical fins resulting in better electrostatic field control over the channel – a crucial advantage determining several unique features of the FinFET device. Particularly, such structure leads to the significant reduction of leakage in off state and helps to suppress other short-channel effects (SCE) intrinsic for planar MOSFET.

B. Device structure and main advantages

A FinFET device structure consisting of 2 fins is shown in Fig. 1. The effective width of one fin in this 3-D device is defined by its geometric parameters: height of the fin (H_{fin}) and width of the fin (W_{fin}) or fin thickness:

$$W_{eff} = 2 \times H_{fin} + W_{fin} \quad (1)$$

The channel length L is defined by a poly gate in a standard way. The geometric parameters are technology-specific and strictly controlled by a foundry.

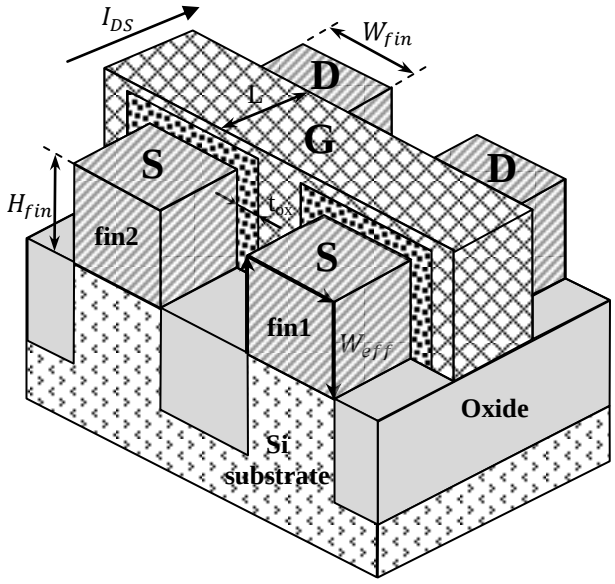

Fig. 1. 2-fins FinFET device structure with geometric parameters

Besides already mentioned advantages the described above 3-D structure of FinFET device has higher integration density providing more performance per linear transistor's width due to vertical channel orientation [6]. Except for leakage savings, lower dynamic power is

achieved at a low operating voltage (from nominal 0.8V down to 0.55V in TSMC 16nm FinFET process) which is a consequence of threshold voltage reduction. As stated in TSMC press releases their 16nm FinFET technology is 50% faster and consumes 60% less power at the same speed in comparison with TSMC's 20nm SoC process [7]. The performance gain is caused by the supreme drive current. It means the FinFET transistors allow to get better performance at defined power consumption or operate equally fast but with much lower power. The flexible trade-off for power, performance, and area (PPA) indicator opens huge opportunities for designers in achieving corresponding targets for different applications.

C. FinFET design challenges overview

Offering a number of advantages, the FinFET technology throws new challenges starting from manufacturing complexities and ending with the thorough sign-off process to address lots of issues including reliability and power integrity. The article is focused on the main features of standard cells design with FinFET technology as an essential part of RTL-to-GDSII digital flow. The most affected on the standard cells FinFET specifics and their impact on the development process are analyzed in Section II. The investigation is done based on TSMC 16nm FinFET technology. Section III presents a description of multi-height layout architecture, its purpose, and features related to the FinFET application. Basic observations and recommendations for layout and circuit design of standard cells including complex functions are given. Section IV demonstrates an example of practical usage of described principles for the development of multi-bit flip-flop cells as part of a standard cell logic library. A comparative analysis of key characteristics of developed cells is provided with respect to analogous cells from a 3rd-party vendor. Final conclusions and outcomes are formulated in Section V.

II. STANDARD CELLS DESIGN CHALLENGES

Standard cell library development is one of the milestones in the SoC design platform deployment for a new technology node. On the one hand, leading IP vendors offer numerous of their design kits including logic libraries and memory compilers for a wide range of technologies. But at the same time their cost can be too high or some additional cells, components are required for specific applications. So in such cases, a problem of internal development of necessary elements is raised [8].

A. Modeling/simulation

From a circuit design standpoint, there are several FinFET features that impact design methodology significantly. The first one is a more complex device model required for simulation. The BSIM4 model used for years is not sufficient to model the 3-D FinFET structure. In response to the issue, a new compact BSIM-CMG (common multi-gate) model was developed by UC Berkeley [9]. But the challenge is mostly related to foundries that are induced to collaborate with model developers and find an effective solution in this area. So, besides the new device model, TSMC has adopted the so-called TSMC Model Interface (TMI) allowing accurate modeling of layout-dependent effects (LDE), NBTI/PBTI aging, and process variation [3].

B. Width quantization

The more vital problem for circuit designers is the so-called width quantization issue [10]. Unlike the planar CMOS process, where the transistor's width is a continuous value (with accuracy to the manufacturing grid), the FinFET device's width is defined according to (1) by the fin's geometric parameters which are process constants. So drive current of the FinFET device can be increased only by constructing parallel multiple fins connected together as shown in Fig. 1 for $nfins$=2. Thus, it implies that for a FinFET, the arbitrary transistor's width is not possible, since it is always a multiple of fin height and the total effective width of the device becomes quantized:

$$W_{total} = W_{eff} \times nfins, \quad (2)$$

where $nfins$ – number of fins in multiple fin device structure. Obviously, the restriction has more impact on analog and memory design rather than digital, but anyway it's a serious obstacle for sizing and optimization when target parameters are critical.

C. RDR and layout granularity

But certainly, the vast majority of challenges for standard cells development with FinFET technology are related to layout design. In case of transition from the planar process, there is almost no possibility to re-use the existing physical design and migrate it to the FinFET technology node due to lots of restricted design rules (RDR).

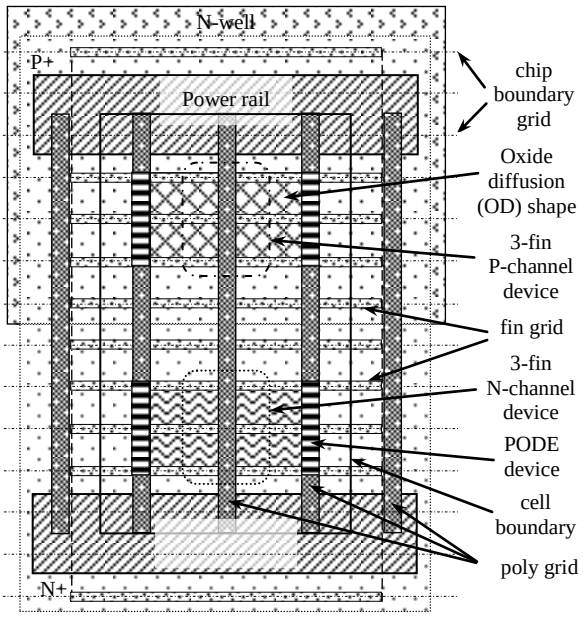

Fig. 2. Simplified layout template of standard cell in FinFET technology

The mentioned above width quantization issue of FinFET devices determines a layout granularity due to the

presence of fin and chip boundary grids (Fig. 2). It implies significant restrictions on the placement of oxide diffusion (OD) regions in cell layout that should be aligned with fin grid:

$$W_{OD} = W_{fin} + grid_{fin} \times (nfins - 1), \qquad (3)$$

where W_{OD} – drawn width of OD shapes, W_{fin} – fin width, $grid_{fin}$ – fin grid value, $nfins$ – number of fins in multiple fin device. At the same time, the top and bottom edges of the cell boundary should be in the chip boundary grid. In case fin and chip boundary grids are equal accurate to some offset as shown in Fig. 2, cell height must be compatible with fin grid. Conventionally cell height was defined by metal routing pitch providing the corresponding number of routing tracks for P&R tools. Now to enable correct abutment of standard cells between neighboring rows in design floorplan and form grid for signal routing cell height has to be chosen as multiple of fin grid and metal pitch [11]. Obviously, there is a more restricted set of cell height values satisfying the condition. So, for TSMC 16nm process cell height values with discrete 1.5 are commonly used (mostly 7.5T, 9T, and 10.5T libraries are included in the IP vendor's offer).

D. Min-jog OD rules

Another limitation related to OD shapes is so-called min-jog rules regulating their form and distance between edges [2]. It impacts the FinFET device sizing strategy and their layout placement since a different number of fins in nearby transistors might result in significant cell area increasing to honor the min-jog OD rules (Fig. 3). For this purpose, it's sometimes reasonable to equalize the number of fins in neighboring transistors to avoid area penalty and other drawbacks if it's allowed by design targets. In other words, it's worth following the layout-driven transistor sizing approach, achieving a compromise between cell characteristics and area.

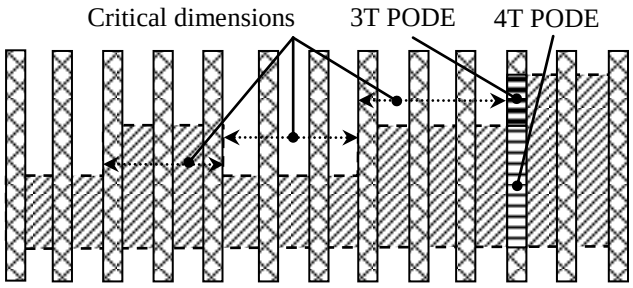

Fig. 3. Min-jog OD rules

E. MEOL

Starting from the 20nm process middle-end-of-line (MEOL) layers are introduced representing a combination of local interconnect (LI or M0) layers between transistor terminals (Front-end-of-line: FEOL) and metal routing (Back-end-of-line: BEOL) [10]. MEOL layers allow to get high-density local routing inside the cell and relieve pin access problems. The connection between FEOL and LI layers is formed by simple overlapping and doesn't require a via. Concerning the FinFET technology process, these are two additional layers known as CA and CB. CA is used to form source/drain connections, while CB is a gate connector.

Presence of MEOL increases both design and fabrication complexity adding tens design rules and new parasitic effects. Thus, the impact of MEOL should be carefully accounted for all design stages since it's one of the dominant sources of parasitic components.

F. PODE

One of the main issues of FinFET technology is edge device degradation [2]. Poly on diffusion edge (PODE) structures form parasitic dummy transistors on OD edges reducing fin stress (Fig. 2). The PODE transistors are active devices that affect circuit parameters and functionality. For this reason, they should be properly processed in physical design to avoid undesirable impact and even functional failures in some cases. There are two basic types of PODE transistors:

- 3-terminal device (3T), formed on OD edges with only one source/drain area. It does not require any special gate connection.
- 4-terminal device (4T) with a floating gate, formed due to abutment of active FinFET transistors. It's unusable from a functional standpoint so the gate should be tied off to power/ground rail depending on transistor type.

Finally, both types of PODE transistors may be formed in case stepped OD shape shown in Fig. 3. The structure results in two parasitic devices sharing the same gate. Meanwhile, the 4T PODE part can be turned into both dummy transistors and regular functional transistors based on design needs.

G. Double patterning

Eventually one of the novelties widely applied in advanced process nodes is related to BEOL constraints. Due to lithography limitations double patterning technique (DPT) is used to split high dense patterns (usually metal layers) into two lower density intermittent patterns represented by two different masks. From a layout design perspective, it implies a coloring concept where shapes of two different colors are associated with two different masks for the same layer formation (Fig. 4).

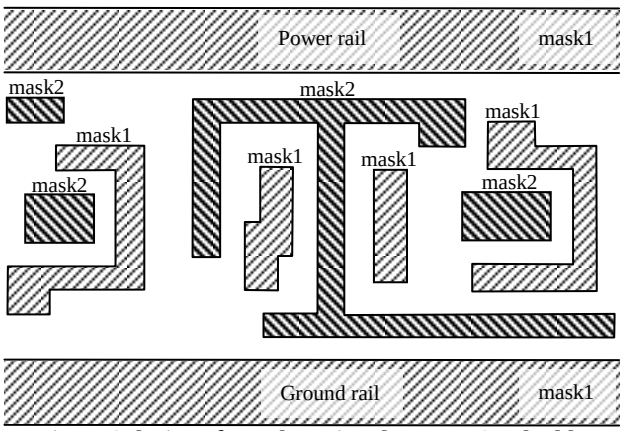

Fig. 4. Coloring of metal routing due to BEOL double patterning

A complication is that there are strict and larger spacing requirements for shapes of the same color which force the layout designer to take care of correct decomposition and coloring of internal metal routing to avoid so-called odd cycle violations. As an example, the same metal shape cannot be continued on nearby track due to larger spacing requirements so only odd or even tracks are available for the same colored nets (Fig. 5). In turn, a coloring of power and ground (P/G) rails is defined usually by cell height and corresponds to the number of routing tracks available. Thus, in case even track library P/G rails should have the same color, while for odd track library the rails to be different colors.

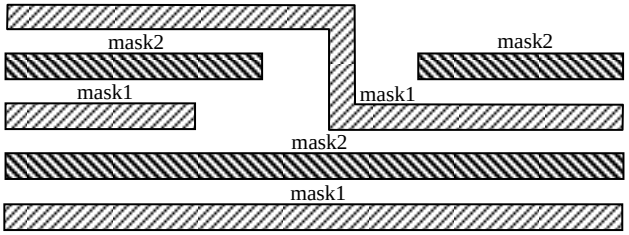

Fig. 5. Example of routing limitation due to DPT

In fact, DPT is used for FEOL and MEOL as well. To minimize spacing all critical layers are processed in two steps: first is forming of basic layer geometry and second is cutting of the shape to make required gaps and generate final geometry. In the 16nm FinFET process the technique is usually applied for OD, poly, and CA layers.

III. MULTI-HEIGHT LAYOUT ARCHITECTURE

Traditionally cell height and layout architecture of standard cell libraries are determined by the target application. To achieve low-power requirements high density or ultra-high density libraries are used for digital design. Regarding TSMC 16nm FinFET process, it implies 7.5T or 9T standard cell layout architecture. So the further discussion will address the 7.5T option as more critical concerning the challenges mentioned above.

Standard cell layout architecture or simply layout template specifies a set of design rules common for all cells in a particular library and ensuring faultless P&R flow on the SoC level. Basically, it includes allowable regions for each layer in relation to the cell boundary, P/G rails specification, requirements for pin shapes and hit points as well as other layout guidelines making all cells in the library unified.

Consider a generalized layout template for FinFET based standard cell. As discovered in the previous section cell height should be in line with the fin grid. In these conditions, it would be highly important to figure out how many routing tracks are available for internal interconnections. As a rule, power/ground rails at the top and bottom of the cell are wide enough to ensure EM/IR requirements, so they remove 1 routing track each. Thus between the rails, there are a few tracks available for internal cell routing, particularly in our case these are 5 tracks only. Meanwhile for complex standard cells with a large number of pins and an intricate system of internal connections larger routing resources are required.

To solve the issue a multi-height or multi-row layout architecture can be applied. Such cells have got shared power and/or ground rails depending on selected type and height equal to even or odd number of row height. Fig. 6 provides a generalized structure of a double-height cell with a shared power rail as the most conventional case. It's not a complete layout and shows only specific objects and layers to support the description below.

Such structure makes available almost twice more routing tracks in comparison with a single-height template. But there is a drawback even for such an approach – now it is necessary to arrange connections between rows inside the multi-height cell. Usually, standard cells utilize Metal1 for internal routing, seldom Metal2 is used in case of a large number of pins and dense routing while higher metals usage is quite undesirable. So having P/G rails in Metal1 and horizontal direction of Metal2 there is no opportunity to use metal layers as inter-row connections. But just here the MEOL layers and poly itself might be used efficiently to resolve the problem. Since CA layer has a vertical direction, it can help to form local interconnections between cell rows (Fig. 6). Such connections should be short enough, as the MEOL layers have higher resistivity, than metals, and may impact the cell parameters noticeably. At the same time, the poly may be naturally used for longer connections, especially as a gate connector.

To ensure that such a cell routing approach is safe in terms of EM and IR drop concerns, a corresponding analysis was done using Voltus-Fi EMIR Self Heating flow. The analysis was run for a wide range of input frequency and output load values at the worst EM/IR conditions (best process, high supply voltage, high temperature). It has shown that internal nets, routed in CA and poly layers, are not in the critical path from an EM/IR standpoint. The EM/IR analysis results showed a significant margin for the nets in comparison with current limits across all kinds of measurements (avg, peak, rms).

The described above approach was successfully applied for complex standard cells development in advanced nodes (e.g. 16nm, 5nm). The efficiency and reliability of the proposed design technique are confirmed by silicon validation results and many company products, which widely used the internally designed standard cells. Based on the experience the following common recommendations for standard cells layout design in advanced nodes can be formulated:

- Multi-height layout architecture should be evaluated and analyzed for complex cells design in the conditions of limited routing resources. Thus, for the high density 7.5T library, there are only 5 tracks available for internal routing, so this is a good candidate to use multi-height layout architecture for cells with a large number of pins/nets.
- Consider layout-driven transistor sizing where it's applicable to get area-efficient cell layouts. In specific practical cases, the approach can provide area benefit up to 10%, but all the changes have to be carefully verified in post-layout simulation to avoid significant degradation of key parameters.

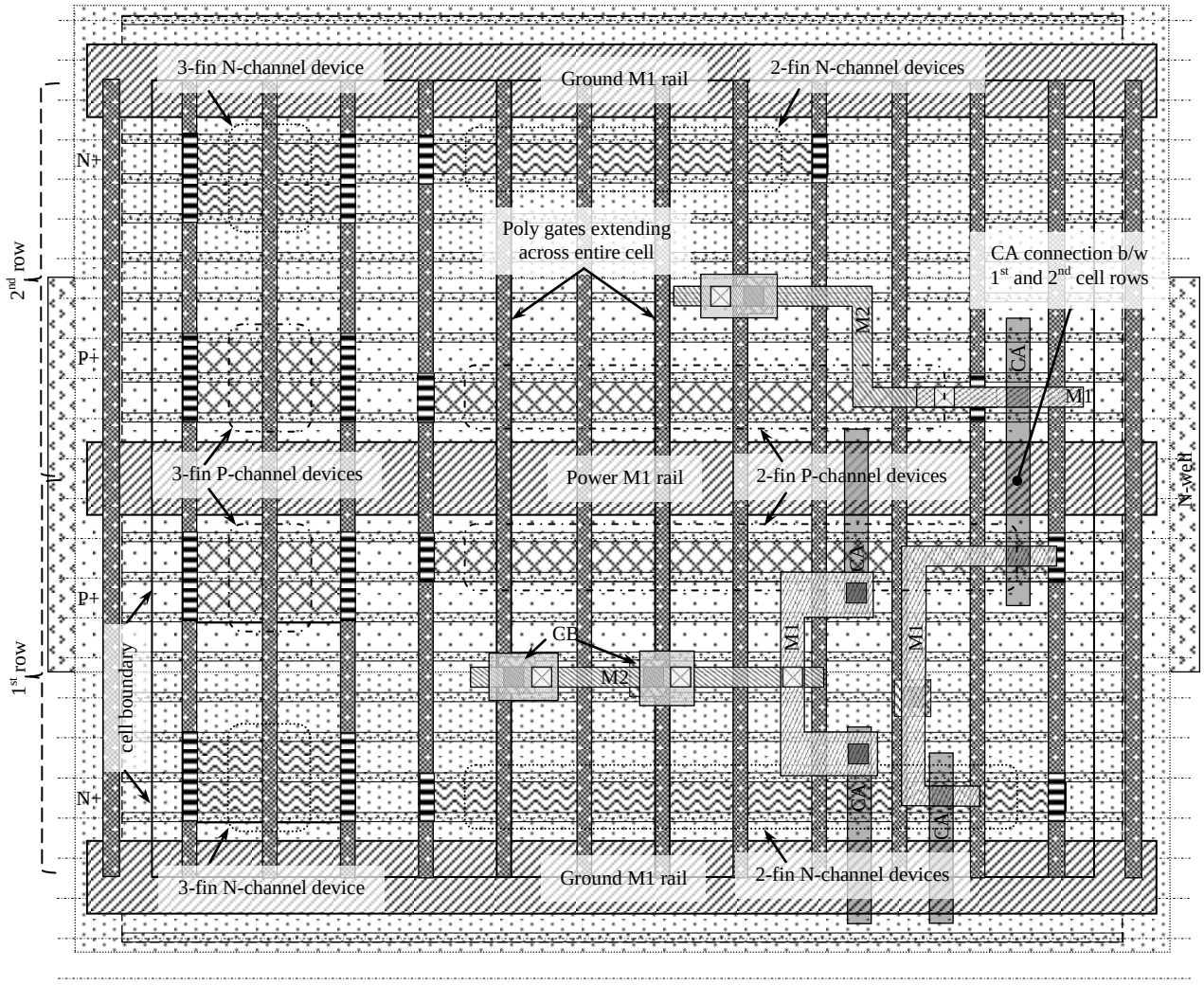

Fig. 6. Generalized structure of double-height cell layout

- Decompose the circuit by separating common parts having the maximum number of connections with other parts of the circuit. Use case of such decomposition is described in the next section of the article based on the example of multi-bit flip-flop cells design.
- Arrange the decomposed parts of the circuit in layout in a way to relieve internal routing. The most conventional principle, also used in this work for multi-bit flip-flop cells development, is to place a common part in the center of the layout having other parts around.
- Use MEOL and poly layers to organize inter-row connections. It allows excluding or reducing usage of higher metals inside complex standard cell layouts, consequently providing more routing resources on the SoC level.

It is worth noting also that layout design time increases significantly for advanced nodes, so it should be taken into consideration in the planning phase of the development (e.g. odd cycle violations correction is very time-consuming).

IV. MULTI-HEIGHT ARCHITECTURE USAGE FOR COMPLEX FUNCTIONAL CELLS DESIGN

Power and area minimization is a conventional goal for most System-on-Chips (SoCs). To meet these requirements, all IP providers started including more complicated solutions in their deliveries which can help to reduce power, area, or both on the SoC level.

Currently, advanced standard cell libraries include complex functional cells. One of the possible solutions to reduce power and area is a multi-bit flip-flop (MBFF) [12]-[14]. At the same time, the multi-bit flip-flop is one of the most complicated cells in standard cell libraries. MBFFs are intended to save power and area in comparison with stand-alone flip-flops (FFs). The main idea of MBFFs usage is to share common resources between all bits. The general concept of MBFF structure is shown in Fig. 7.

Every stand-alone flip-flop contains master and slave latches, clock elements to generate internal clock signals with required polarity, initialization elements to generate internal Set/Reset signals with required polarity depending on specified functionality, auxiliary elements to enable scan ability of flip-flop.

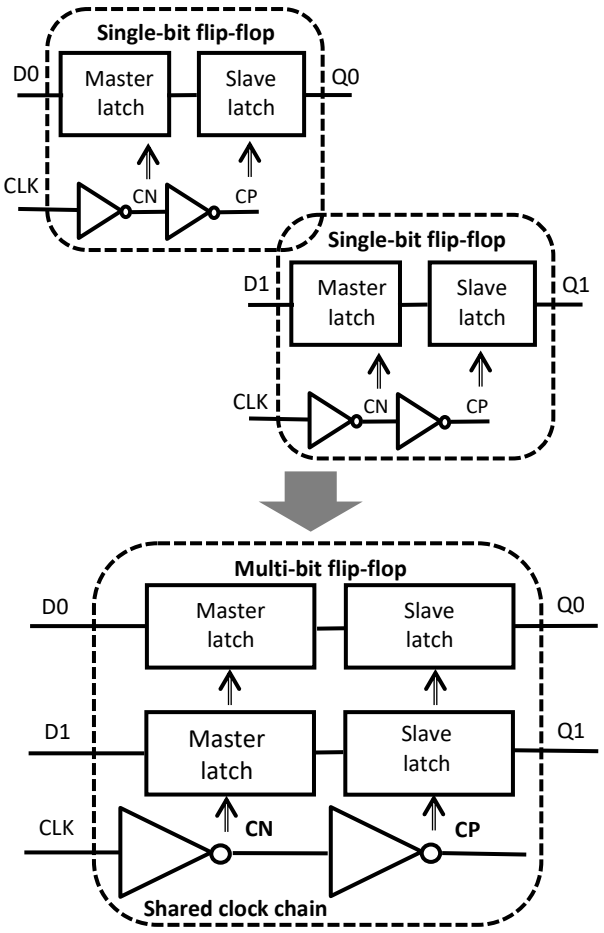

Fig. 7. General circuit architecture of multi-bit flip-flop

Let's consider in more detail what benefits the MBFF structure has in comparison with single-bit FFs.

The internal clock chain (conventionally, it includes two clock inverters) makes a significant contribution to total power for every flip-flop [15]. MBFF structure allows avoiding clock elements duplication in clock chain that reduces total power. Thus, the MBFF structure has shared clock elements that can drive more than one flip-flop.

Another advantage of the MBFF structure is area reduction due to the following reasons:

- clock chain is shared between all bits of MBFF instead of availability in every single-bit FF;
- initialization logic (Set/Reset chains, which generate direct and inverted signals) is also shared between all bits of MBFF instead of availability in every single-bit FF;
- simple circuitry, which generates direct and inverted scan enable internal signals for scannable flip-flops, can be also shared between all bits of MBFF.

There is one more indirect and potential advantage of multi-bit flip-flops, which give more benefit on the higher SoC level. The MBFF structure might have an embedded scan chain, which is properly verified during the cell development stage. That means there will be no need to fix hold violations for MBFFs, which might happen during SoC logic synthesis.

To summarize, we can conclude that multi-bit flip-flops are the power effective and area-effective solutions. At the same time, SoC designers should consider the fact, that MBFFs have some timing degradation in comparison with single-bit versions.

The described above multi-height layout architecture and proposed recommendations were effectively applied for MBFF layout design. The MBFF circuit is decomposed based on the circuit structure listed above: the shared logic for clock chain, initialization signals, and control scan logic represent a common part, that is placed in the center of the layout. Separate flip-flop parts, which correspond to each bit in MBFF structure, are placed around to arrange effective routing. Poly gates extending across the entire cell height are used to distribute direct and inverted clock signals. CA layer can be efficiently applied to organize internal scan chain between bits in MBFF structure.

Typically, standard cell libraries include multi-bit flip-flops up to 8-bits. During power optimization on the SoC level, a substantial part of single-bit flip-flops is grouped and replaced by the corresponding multi-bit flip-flops. To provide flexibility for optimization tools at this stage, the multi-bit flip-flops are developed having different bit-depth and driving strengths. Thus, in our library 2-bit, 4-bit, and 8-bit flip-flops with several driving strengths are presented.

To estimate the benefits that can be achieved, a cell-level benchmark, comparing the main characteristics of the developed multi-bit flip-flops with reference data for single-bit flip-flops, was done. Trend analysis and comparison results for multi-bit flip-flops with equivalent numbers of single-bit flip-flops are given in Table 1.

Table 1

Comparison: one N-bit MBFF versus N standalone FFs

	Timing (Max setup + Max delay)	**Total power**	**Area**
1-bit	reference		
2-bit	+ 19.7%	-6.2%	-14.3%
4-bit	+ 23.7%	-16.8%	-21.4%
8-bit	+26.7%	-21.7%	-23.2%

Three main characteristics were compared:

- Timing: the sum of maximum setup time and maximum delay time were defined and compared for single-bit flip-flop and the corresponding 2-bit, 4-bit, and 8-bit flip-flops;
- Power: total power for 2-bit, 4-bit, and 8-bit multi-bit flip-flops was defined and compared with the equivalent number of single-bit flip-flops (e.g. total power for 2-bit multi-bit flip-flop was compared with power values of 2 single-bit flip-flops, etc.)
- Area: a total area for 2-bit, 4-bit, and 8-bit multi-bit flip-flops was defined and compared with the equivalent number of single-bit flip-flops (similar, e.g. total area for 2-bit multi-bit flip-flop was compared with area values of 2 single-bit flip-flops, etc.)

These results confirm power and area efficiency of MBFFs usage.

Complex cells in standard cell libraries cannot have an infinite length within one row as for every technology there is a limit for X-size of layouts (basically due to latch-up rules). Therefore, such complicated cells can have multi-row architecture. As an example, depending on cell complexity, it can be 2-rows or 4-rows. Using multi-row architecture and effective layout implementation methods from chapter 3, several MBFF families for the internal 16nm FinFET standard cell library were developed.

The results of selective cell-level comparison of internally-developed versus vendor-provided 4-bit flip-flops are given in Table 2.

Table 2

Cell-level comparison: 4-bit MBFF internally developed versus external vendor

	Internally developed	**External vendor**	**Difference**
Layout architecture	2-rows	1-row	-
Area, um^2	4.06	4.19	-3.1%
Total power, uW	9.23	10.28	-10.1%
Timing, ps (Max delay + Max setup)	137.24	137.16	<0.1%
Max hold value, ps	14.5	16.5	-12.1%
Routability (Metal 2 tracks used per row)	4.5	5	-

Presented results show that multi-row architecture and effective layout implementation methods in 16nm technology provide better area (~3%), better total power (~10%), while keeping about the same performance (the difference is less than 0.1%), and having better hold timing parameter (~12%). Also, multi-row architecture provides additional benefits in terms of routability as the number of occupied metal tracks per row, used for internal cell routing, is less. Thus, multi-row architecture provides more available metal tracks for routing on the SoC level.

V. CONCLUSION

Main specifics and challenges for standard cell design in FinFET technology have been overviewed in this article.

Multi-height or multi-row layout architecture for complex cells design in 16nm FinFET technology has been presented. The set of guidelines and recommendations for complex multi-row cells with respect to layout design has been formulated.

Based on the proposed recommendation a number of complex multi-row multi-bit flip-flops have been developed for the 16nm FinFET standard cell library. The multi-bit flip-flops are fully consistent and can be used together with the existing cells. The cell-level benchmark for newly developed cells has been done. The results of comparison have shown better PPA characteristics on the cell level, which was also proven by silicon results. Guidelines presented in this article can be applied by standard cell developers for the design of area-effective complex cells with multi-row layout architectures.

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Особенности проектирования сложных стандартных ячеек в передовых FinFET технологиях

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***Аннотация* — Продолжающееся масштабирование размеров планарной КМОП технологии ведет к разработке новых методов для глубоко-субмикронных передовых процессов. Технология полевого транзистора с трехмерной структурой в форме плавника (Fin Field-Effect Transistor, FinFET) становится одним из главных направлений при переходе к нормам проектирования 16нм и ниже. Предоставляя ряд возможностей и преимуществ для разработки ИС FinFET технология поднимает множество вопросов относительно применения имеющихся методологий, средств и маршрутов проектирования. В то время как производители САПР не предлагают каких-либо абсолютно инновационных подходов к разработке СнК для передовых процессов, FinFET технология должна быть эффективно адаптирована к существующим маршрутам проектирования с учетом ее особенностей. Данная статья включает обзор основных проблем использования технологии FinFET 16нм при разработке библиотек стандартных ячеек, являющихся неотъемлемой частью любого цифрового маршрута проектирования. Сформулированы общие рекомендации при проектировании стандартных ячеек в FinFET технологии, а также представлены особенности разработки сложных ячеек с применением многорядной топологической архитектуры. Предложенные рекомендации опробованы на примере разработки многоразрядных триггеров, обеспечивающих эффективное, с точки зрения занимаемой площади, решение для малопотребляющих приложений.**

***Ключевые слова* — FinFET технология, передовой процесс, цифровая библиотека, библиотека стандартных ячеек, логическая библиотека, малопотребляющая стандартная ячейка, многорядная топологическая архитектура, многоразрядный триггер.**

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